cooling step was noted as providing advantages disclosed in the specification that were not recognized by the cited prior art.

The current Office Action responds by citing language in Papasouliotis, in U.S. Pat. No. 5,316,278 ("Sherstinsky"), in U.S. Pat. No. 6,310,755 ("Kholodenko"), and in Wang. In addition, a separate rejection of Claims 17 and 20 has been set forth under §103 that relies on Wang in addition to Hong and Papasouliotis. None of these citations corrects the previous deficiency in setting forth a *prima facie* case since each of them still fails to provide documentary support drawn from the dep/etch/dep art for disclosing the cooling step.

First, the following language was cited from Papasouliotis:

> [T]ransitions from a deposition to an etching step are effected by varying the composition of the mixture, the power supplied to the wafer, the chamber pressure, and/*or* the temperature of the wafer.
> (Papasouliotis, Col. 8, ll. 42 – 45, emphasis added).

This language merely states that the deposition and etching steps are characterized by differences in various process conditions, one of which *might* include temperature ("and/*or*"). The plain language explicitly contemplates that no change in temperature might be made, if other process conditions are changed to effect an etching step. Accordingly, the statement in the current Office Action that Papasouliotis expresses "the *need* to alter temperature before the transition from deposition to etching" (emphasis added) is simply incorrect. Also, the Office Action concedes that Papasouliotis "do[es] not explicitly disclose that the changing of temperature would be a cooling step" (Office Action, p. 4), indicating that such cooling is "inherent" because of etch sensitivity to temperature (*id.*, p. 5). This is a misapplication of the doctrine of inherency, which requires that the inherent element *necessarily* be present (MPEP 2112); in contrast, as just noted, the language in Papasouliotis contemplates that etching may be performed without *any* change in temperature.

Furthermore, the cited language specifically teaches a continuous "transition" from a deposition step to an etching step. As such, it very directly teaches away from the claim limitation requiring a separate step between the first deposition and etching, as embodied by the "thereafter" language in steps (c) and (d) of independent Claim 17 or in steps (iii) and (iv) of independent Claim 20. Such teaching away has long been recognized as strong evidence that the suggested modification is *not* obvious.

Second, the following language was cited from Sherstinsky:

> In the plasma etching of semiconductor wafers, it is conventional to cool the wafer (*or more properly to maintain it at a preselected temperature*) during the etch process by flowing a gas, e.g., helium or argon, through an opening in the underlying cathode support pedestal to the space between the top surface of the pedestal and the undersurface (backside) of the wafer. The presence of such a gas in this space serves t[o] enhance the thermal coupling of the wafer to the underlying pedestal which serves to cool the wafer, i.e. *to maintain it at a preselected temperature* despite heat generated by the plasma etching being carried out on the top surface of the wafer. (Sherstinsky, Col. 1, ll. 15 – 26, emphasis added).

This language makes it unmistakably clear that Sherstinsky is referring to "cooling" merely to counteract the plasma heat, but is intending to maintain a constant temperature of the wafer during etching. This is completely unlike the claim limitation which uses language ("thereafter" in elements (c) and (d) of Claim 17 and in elements (iii) and (iv) of Claim 20) to demarcate the cooling step from the etching step, and refers instead to a deliberate lowering of the temperature (*see* Application, p. 20, ll. 11 – 14). It is hoped that clarification of this semantic difference makes clear that the claim limitation has nothing to do with maintaining a constant temperature during etching as described in Sherstinsky.

Third, the following language was cited from Kholodenko:

> In certain processes, it is also desirable to rapidly cool the substrate *in order to maintain the substrate in a narrow range of temperatures*, especially for etching interconnect lines that have very small dimensions and are positioned close together.
> (Kholodenko, Col. 1, ll. 56 – 60, emphasis added).

The emphasized language makes it clear that Kholodenko is referring to "cooling" in the same sense as Sherstinsky — an approximately constant temperature is being maintained during the etching step. There is no disclosure of a separate step that deliberately lowers the temperature between deposition and etching phases of a dep/etch/dep process.

Fourth, the following language was cited from Wang:

> Therefore, the inventive process comprises insulating these lines by a two step HDP-CVD process wherein each step simultaneously deposits and etches a dielectric material such as silicon dioxide. The first step is performed with a low deposition-to-sputtering ratio (D/S) of 2 to 4 and Helium backpressure of 8 inner and 10 outer Torr. Subsequently there is a period of time where no

> deposition or etching as allowed and the wafer is subjected to a cooling by applying a stream of inert gas to the backside of the wafer. After this treatment the deposition/sputtering is resumed with a D/S of 4 to 6 and a Helium backpressure of 6 inner and 10 outer Torr. In this manner the temperature of the metallurgy lines is maintained below a point that would cause distortion of the lines, specifically no "hillocks" are formed.
> (Wang, Col. 5, ll. 8 – 22).

The Office Action characterizes Wang as disclosing "multiple dep/etch steps to fill dielectric gaps" with a "cooling step after a deposit step" (Office Action, p. 5) and explicitly relies on this disclosure for the cooling step in the §103 rejections of Claims 17 and 20 (*id.*, p. 4). This characterization is misleading because Wang is not directed to a dep/etch/dep process; the "dep/etch" steps that are referred to are, in fact, deposition steps that include a sputtering component from the HDP process, as do virtually all HDP deposition processes. That they are both properly identified as deposition steps is evident from the explicit D/S ratios,[1] which are greater than 1 in both instances. Since Wang does not discuss the use of an etching step at all, it is not relevant to the claim limitations.

In fact, the second deposition step in Wang has a higher D/S ratio than does the first deposition step (4 – 6 for the second versus 2 – 4 for the first). Accordingly, the cooling that Wang teaches follows a step having a lower deposition component and precedes a step having a greater deposition component. This is completely opposite to what is claimed. The claim language requires a specific order of steps with the cooling occurring after a step having a greater deposition component and preceding a step having so low a deposition component that it is described as an etching step. If anything, Wang teaches cooling between steps that exhibit an *increase* in rate of deposition over time. This is in marked contrast to the claim recitation of cooling between steps that correspond to a decrease in rate of deposition over time. Thus, again, the cited reference teaches away from the claim limitations, a factor that strongly indicates *against* a §103 rejection.

To summarize, none of the additional references cited in response to Applicants assertion that no documentary support had been provided from the dep/etch/dep art for the cooling step remedies that deficiency. The cited references are not drawn from the dep/etch/dep art, refer to "cooling" in a manner completely unlike that claimed, or teach away from the cooling limitation as it is recited in the claims.

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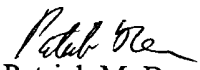
[1] Both Wang and the Application use the same definition for D/S. *Compare* Wang, Col. 6, ll. 21 – 24 with Application, p. 16, ll. 12 – 15.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,



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